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SQUIRE, SANDERS & DEMPSEY L.L.P.
8000 TOWERS CRESCENT DRIVE
14TH FLOOR
VIENNA, VA 22182-6212

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NG, CHRISTINE Y	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/492,265	HAO ET AL.	
	Examiner	Art Unit	
	CHRISTINE NG	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 line 3: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

In claim 8 line 3: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

In claim 13 line 5: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

In claim 28 line 3: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

In claim 32 line 5: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

Claim 34 recites the limitation "the memory block" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

In claim 52 line 3: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

In claim 57 line 4: It is unclear what "a location" is used to store. It is interpreted as storing a received packet.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 8-11, 13-15, 18-21, 23-25, 28-30, 32-34, 37-40, 42-44, 47-50, 52-55, and 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,386,413 to McAuley et al in view of U.S. Patent No. 6,279,097 to Kaku, and in further view of U.S. Patent No. 6,021,132 to Muller et al.

Referring to claims 1 and 28, McAuley et al disclose in Figure 5 a memory structure (memory 100) comprising:

An Address Resolution Table (CAM's 1-3) for resolving addresses in a packet-based network switch (Figure 3) and using a key to index a location within the Address Resolution Table, wherein the key is a packet destination address. CAM's 1-3 reads a destination address of a received packet, and matches the destination address with destination addresses stored in the routing table entries of the CAM's. When a match is found, the CAM's output a corresponding output port entry associated with the matching destination address. Refer to Column 6, line 59 to Column 7, line 35.

A Packet Storage Table (RAM) , the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected

portion of memory with the Address Resolution Table. Memory 100 can also include a RAM for storing packet data. Refer to Column 10, lines 31-45.

A mechanism configured to receive an individual packet for enabling only one transmit descriptor (memory address) read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted. When a match occurs between a received destination address and a destination address in the routing table of the CAM's, a memory address is read. The memory address corresponds to the location of the stored packet data in the RAM. Refer to Column 10, lines 31-45.

McAuley et al do not disclose wherein the key *is a predefined portion* of a packet destination address.

Kaku discloses a system wherein a controller extracts an incoming packet's destination address, matches the address with one of the addresses stored in an address lookup table, and reads a corresponding output port. The entire 48-bit destination address is not used in the address lookup table. Instead, memory locations in the address lookup table are addressed by a portion of the destination address in order to save space. Refer to Column 1, line 60 to Column 2, line 32. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the key *is a predefined portion* of a packet destination address. One would have been motivated to do so to reduce the lookup table to a smaller and more practical size.

McAuley et al also do not disclose a *single buffer per packet* mechanism.

Muller et al disclose in Figure 3A a shared memory 230 with a plurality of buffers for storing packets. A given packet's data can be stored in multiple buffers. However, it may be convenient to limit packet data contained within a particular buffer to one packet. Refer to Column 8, lines 37-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a *single buffer per packet* mechanism. One would have been motivated to do so in order to prevent mixing of more than one packet within a buffer, thereby simplifying the system.

Referring to claim 2, McAuley disclose in Figure 5 a Transmit Descriptor Table (table storing destination addresses corresponding to RAM memory addresses and output ports) being associated with a corresponding packet-based network transmit port. Refer to Column 7, line 8 to Column 8, line 20; and Column 10, lines 31-45.

McAuley et al do not disclose a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

Muller et al disclose in Figures 3A and 3B a shared memory manager 220 that manages the shared pool of free buffers in shared memory 230. Shared memory manager 220 returns buffers to the free pool once an output port 206 has finished transmitting packet data from the buffer. Each buffer may be of the same size with a predetermined number of memory lines for storing packet data. Refer to Column 7, lines 20-28 and Column 8, lines 22-51. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-

determined number of memory locations associated therewith. One would have been motivated to do so to allow for dynamic buffer allocation and re-use of free buffers.

Referring to claim 3, McAuley et al do not disclose wherein the packet- based network switch implements an IEEE standard 802.3 communication protocol.

Muller discloses in Figure 1 a similar switching system which uses the IEEE standard 802.3 protocol. Refer to Column 3, lines 54-63 and Column 4, lines 39-60. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the packet-based network switch implements an IEEE standard 802.3 communication protocol. One would have been motivated to do so in order to utilize the Ethernet protocol for data transmission in LAN's.

Referring to claim 4, McAuley et al disclose in Figure 3 wherein the switch (50) comprises plural ports (51-1 to 51-n, 52-1 to 52-n). Refer to Column 1, lines 50-58.

Referring to claim 5, McAuley et al do not specifically disclose wherein the switch comprises at least 8 ports. However, as shown in Figure 3, switch 50 can have up to n ports, which includes 8.

Referring to claim 6, McAuley et al disclose in Figure 3 wherein an associative memory structure comprises one of an n-way associative memory (one-way associative memory: each address corresponds to one output port in each CAM), a hash table (none), a binary search structure (none), and a sequential search structure (none). Refer to Column 7, lines 8-35; and Column 8, line 51 to Column 9, line 43.

Referring to claim 8, McAuley et al disclose in Figure 5 a memory structure (memory 100) comprising an Address Resolution Table (CAM's 1-3) having an

associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch (Figure 3) and using a key to index a location within the Address Resolution Table, and a mechanism configured to receive an individual packet for enabling only one transmit descriptor (memory address) read per said individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key, wherein the entire packet is to be transmitted, wherein the key is a packet destination address. CAM's 1-3 reads a destination address of a received packet, and matches the destination address with destination addresses stored in the routing table entries of the CAM's. When a match is found, the CAM's output a corresponding output port entry associated with the matching destination address. Refer to Column 6, line 59 to Column 7, line 35. Also, when a match is found, a memory address is read. The memory address corresponds to the location of the stored packet data in a RAM. Refer to Column 10, lines 31-45.

McAuley et al do not disclose wherein the key *is a predefined portion* of a packet destination address. Refer to the Kaku et al rejection part of claims 1 and 28.

McAuley et al also do not disclose a *single buffer per packet* mechanism. Refer to the Muller et al rejection part of claims 1 and 28.

Referring to claim 9, McAuley et al disclose in Figure 5 a Packet Storage Table (RAM), the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value. Memory 100 can also include a RAM for storing the packet data. Refer to Column 10, lines 31-45. As shown in Figure 2, a packet includes address data and user data. Refer to Column 1, lines 35-43.

Referring to claim 10, McAuley et al disclose in Figure 5 a Transmit Descriptor Table (table storing destination addresses corresponding to RAM memory addresses and output ports), the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address (each CAM 1-3 is identified by a different mask circuit 120-122) and a Table Descriptor Value (each CAM 1-3 has different stored destination addresses, as shown by Table 3). Refer to Column 7, line 8 to Column 8, line 20; and Column 10, lines 31-45.

Referring to claim 11, McAuley et al disclose in Figure 5 wherein the associative memory structure comprises one of a direct-mapped/one-way associative memory structure (one-way associative memory: each address corresponds to one output port in each CAM) and a two-way associative memory structure (none). Refer to Column 7, lines 8-35; and Column 8, line 51 to Column 9, line 43.

Referring to claims 13 and 32, refer to the rejection of claims 1 and 28; claim 8; claim 9; and claim 10.

Referring to claims 14 and 33, refer to the rejection of claim 6.

Referring to claims 15 and 34, McAuley et al disclose in Figure 5 wherein the memory block comprises a shared memory block. The RAM is a shared memory block since it holds many packets to different destinations. Refer to Column 10, lines 31-45.

Referring to claims 18 and 37, refer to the Muller et al rejection part of claim 2.

Referring to claims 19 and 38, McAuley et al do not disclose wherein the Free Buffer Pool further comprises a buffer control memory.

Muller et al disclose in Figures 3A and 3B a shared memory manager 220 that manages the shared pool of free buffers in shared memory 230. Shared memory manager 220 returns buffers to the free pool once an output port 206 has finished transmitting packet data from the buffer. Refer to Column 7, lines 20-28 and Column 8, lines 22-51. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the Free Buffer Pool further comprises a buffer control memory. One would have been motivated to do so in order to provide a means to control dynamic buffer allocation.

Referring to claims 20 and 39, McAuley et al do not disclose wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

Muller et al disclose in Figures 3A and 3B a shared memory manager 220 that has a count array 430 for managing the shared pool of free buffers in shared memory 230. The location of a given count field in the count array 430 represents the start address of the corresponding buffer in the shared memory 230. Also, the shared memory 230 is made up of a plurality of buffers; each of the buffers may be of the same size. Refer to Column 8, lines 37-51; and Column 9, line 65 to Column 10, line 7. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the

pre-determined number of buffer pool memory locations. One would have been motivated to do so in order to locate and address of the buffers in the shared memory.

Referring to claims 21 and 40, McAuley et al disclose in Figure 5 wherein at least two of the Address Resolution Table (CAM's 1-3), the Transmit Descriptor Table (table storing destination addresses corresponding to RAM memory addresses and output ports), the Packet Storage Table (RAM), and the Free Buffer Pool (none) share a memory block (memory 100). CAM's 1-3, table storing destination addresses corresponding to RAM memory addresses and output ports, and RAM are located within memory 100.

Referring to claims 23 and 42, McAuley et al do not disclose a free buffer manager, including: a buffer bus controller; a buffer bus register; a buffer control finite state machine, operably coupled with the bus controller and the bus register; and a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

Muller et al disclose in Figures 3B and 4 a free buffer manager (shared memory manager 220), including: a buffer bus controller (pointer RAM 320); a buffer bus register (arbiter 470); a buffer control finite state machine (array controller 450), operably coupled with the bus controller and the bus register; and a buffer search engine (address/data generator 460), operably coupled with the bus controller, bus register, and finite state machine. Pointer RAM 320 controls the buffers by storing usage counts for buffers, arbiter 470 arbitrates among the ports to provide only a single port with access to the pointer RAM 320, array controller 450 schedules read and write

operations for the pointer RAM 320, and address/data generator 460 provides addressing into pointer RAM 320. Refer to Column 9, line 5 to Column 10, line 45. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a free buffer manager, including: a buffer bus controller; a buffer bus register; a buffer control finite state machine, operably coupled with the bus controller and the bus register; and a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine. One would have been motivated to do so to provide means to control the shared buffer for dynamic buffer allocation.

Referring to claims 24 and 43, McAuley et al do not disclose wherein the buffer bus controller comprises: a buffer free bus controller for detecting a buffer request and presenting the request to at least one of the finite state machine and the buffer search engine; and a buffer grant bus controller for granting an available free buffer, as indicated by the buffer, as indicated by the buffer bus register.

Muller et al disclose in Figures 3B and 4 wherein the buffer bus controller (pointer RAM 320) comprises: a buffer free bus controller (count array 430) for detecting a buffer request and presenting the request to at least one of the finite state machine and the buffer search engine; and a buffer grant bus controller (tag array 420) for granting an available free buffer, as indicated by the buffer, as indicated by the buffer bus register. Count array 420 stores a count representing ports that are currently using a corresponding buffer in the shared memory 230, and tag array 420 indicates the availability of buffers that can be granted for use. Refer to Column 9, line 65 to Column 10, line 20. Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to include wherein the buffer bus controller comprises: -a buffer free bus controller for detecting a buffer request and presenting the request to at least one of the finite state machine and the buffer search engine; and a buffer grant bus controller for granting an available free buffer, as indicated by the buffer, as indicated by the buffer bus register. One would have been motivated to do so to provide means to control the request and granting of free buffers.

Referring to claims 25 and 44, McAuley et al do disclose wherein the buffer search engine comprises a pipelined buffer search engine.

Muller et al discloses in Figures 3B and 4 that the buffer search engine (address/data generator 460) comprises a pipelined buffer search engine since it generates signals for the memories of the pointer RAM 320 to modify the count and tag fields, which reflect the buffer ownership. Refer to Column 10, lines 28-35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the buffer search engine comprises a pipelined buffer search engine. One would have been motivated to do so in order to provide a means to control dynamic buffer allocation.

Referring to claims 29 and 47, refer to the rejection of claim 3.

Referring to claims 30 and 48, refer to the rejection of claim 4.

Referring to claim 49, McAuley et al do not specifically disclose wherein the switch comprises at least 4 ports. However, as shown in Figure 3, switch 50 can have up to n ports, which includes 4.

Referring to claim 50, refer to the rejection of claim 5.

Referring to claims 52 and 57, refer to the rejection of claims 1 and 28; and claim 6.

Referring to claims 53 and 60, refer to the rejection of claim 4.

Referring to claim 54, refer to the rejection of claim 49.

Referring to claim 55, refer to the rejection of claim 5.

Referring to claim 58, McAuley et al disclose in Figure 5 wherein the direct-mapped/one-way associative memory is searched using a destination address key direct-mapped address search. CAM's 1-3 each use a one-way associative memory structure since each possible destination address corresponds to one output port in each CAM. Refer to Column 7, lines 8-35; and Column 8, line 51 to Column 9, line 43.

Referring to claim 59, refer to the rejection of claim 3.

5. Claims 7, 12, 22, 31, 41, 51 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,386,413 to McAuley et al in view of U.S. Patent No. 6,279,097 to Kaku in view of U.S. Patent No. 6,021,132 to Muller et al, and in further view of U.S. Patent No. 5,765,036 to Lim.

Referring to claims 7, 12 and 31, McAuley et al do not disclose wherein the number of memory accesses required per Ethernet frame is one of: one cycle per frame for address resolution; one cycle per frame for address learning; one cycle per frame for transmission read; one cycle per frame for transmission write; one cycle per eight bytes for a frame data read; and one cycle per eight bytes for a frame data write.

Lim discloses a shared memory device which allows for one system to write data to a memory location in one cycle and another system to read the data on the next data

transfer cycle. This allows for maximum flexibility in a system using a shared memory. Refer to Column 8, lines 22-39. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the number of memory accesses required per Ethernet frame is one of: one cycle per frame for address resolution (none); one cycle per frame for address learning (none); one cycle per frame for transmission read; one cycle per frame for transmission write; one cycle per eight bytes for a frame data read (none); and one cycle per eight bytes for a frame data write (none). One would have been motivated to do so to write data in one cycle and read data in the following cycle, thereby allowing for fast data transfer.

Referring to claims 22, 41, 51 and 56, McAuley do not disclose wherein a packet-based network switch implements an IEEE Standard 802.3 communication protocol. Refer to the Muller et al rejection part of claim 3.

McAuley et al also do not disclose wherein the number of memory accesses required per Ethernet frame is one of: one cycle per frame for address resolution; one cycle per frame for address learning; one cycle per frame for transmission read; one cycle per frame for transmission write; one cycle per eight bytes for a frame data read; and one cycle per eight bytes for a frame data write. Refer to the rejection of claims 7, 12 and 31.

6. Claims 16, 17, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,386,413 to McAuley et al in view of U.S. Patent No. 6,279,097 to Kaku in view of U.S. Patent No. 6,021,132 to Muller et al, and in further view of U.S. Patent No. 6,088,793 to Liu et al.

McAuley et al do not disclose wherein the Transmit Descriptor Table comprises a FIFO memory structure (claims 16 and 35), and wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and tail memory pointer (claims 17 and 36).

Liu et al disclose in Figure 4 line address buffer LAB 230 which is a circular FIFO buffer with 16-20 entries, a head pointer and a tail pointer. Entries are deallocated by indexing the tail pointer of the FIFO so the first arriving packets are transmitted first. Refer to Column 4, line 55 to Column 6, line 3. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the Transmit Descriptor Table comprises a FIFO memory structure (claims 16 and 35), and wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and tail memory pointer (claims 17 and 36). One would have been motivated to do so in order to allow the first arriving packet in the memory structure to be serviced first and to utilize the pointers to determine packet service order in the memory structure.

7. Claims 26, 27, 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,386,413 to McAuley et al in view of U.S. Patent No. 6,279,097 to Kaku in view of U.S. Patent No. 6,021,132 to Muller et al, and in further view of U.S. Patent No. 5,940,375 to Soumiya et al.

Referring to claims 26 and 45, McAuley et al do not disclose wherein the buffer bus register comprises a LIFO.

Soumiya et al disclose in Figure 4 a system wherein quality class queues 409 are inside a common buffer 406 that make up a LIFO buffer. Refer to Column 18, lines 44-52. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include wherein the buffer bus register comprises a LIFO. One would have been motivated to do so in order to allow the top of the buffer to be serviced first.

Referring to claims 27 and 46, McAuley et al do not disclose wherein the LIFO comprises an eight-location LIFO. However, the LIFO disclosed in Soumiya et al can contain any number of locations to store packets, including eight.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINE NG whose telephone number is (571)272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571) 272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C. Ng
May 3, 2008

/FIRMIN BACKER/
Supervisory Patent Examiner, Art Unit 2616